

UNITED STATES PATENT AND TRADEMARK OFFICE



UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO |
|--|-----------------|----------------------|---------------------|-----------------|
| 10/733,038 | 12/11/2003 | Theodore W. Houston | TI-35881 | 8454 |
| 23494 | 7590 12/09/2004 | | EXAMINER | |
| TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265 | | | LE, THON | IG QUOC |
| | | | ART UNIT | PAPER NUMBER |
| , | | | 2818 | <u> </u> |

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | Application No. | Applicant(s) | | | |
|--|--|----------------------|--|--|--|--|
| Office Action Summary | | 10/733,038 | HOUSTON, THEODORE W. | | | |
| | | Examiner | Art Unit | | | |
| | | Thong Q. Le | 2818 | | | |
| The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply | | | | | | |
| A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). | | | | | | |
| Status | · | | | | | |
| 1) | Responsive to communication(s) filed on | | | | | |
| 2a)[| This action is FINAL . 2b)⊠ This | action is non-final. | | | | |
| 3) | 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. | | | | | |
| Disposition of Claims | | | | | | |
| 4) Claim(s) 1-21 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 1-5,8-10 and 12-21 is/are rejected. 7) Claim(s) 6,7 and 11 is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. | | | | | | |
| Applicati | ion Papers | | | | | |
| 9) The specification is objected to by the Examiner. | | | | | | |
| 10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner. | | | | | | |
| | Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). | | | | | |
| Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. | | | | | | |
| Priority (| under 35 U.S.C. § 119 | | | | | |
| 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. | | | | | | |
| Attachmen | nt(s) | | | | | |
| 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) | | | | | | |
| 3) Infor | ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) er No(s)/Mail Date | | ail Date nal Patent Application (PTO-152) | | | |

DETAILED ACTION

1. Claims 1-21 are presented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Duplicate Claim

3. Applicant is advised that should claim 4 be found allowable, claim 3 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

With understanding of examiner, the function of claims 3 and 4 are the same.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

Application/Control Number: 10/733,038

Art Unit: 2818

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5,8-10,12-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomotani (U.S. Patent No. 6,188,628).

Regarding claims 1, 12, Tomotani discloses an SRAM device ((Figure 1), comprising:

an SRAM array (1) coupled to row peripheral circuitry (3) by a word line (WL) and coupled to column peripheral circuitry (3) by bit lines (BL); and

an array low voltage control circuitry (Figure 7) that provides an enhanced low operating voltage V_Ess to said SRAM array during at least a portion of an active mode thereof (Column 11, lines 46-67, Column 12, lines 1-4).

Regarding claims 2-5, 12-21, Tomotani discloses wherein the array low voltage control circuitry provides said enhanced low operating voltage Vess only during a WRITE operation (Figur2, Figure 7, Column 7, lines 4-18, Column 9, lines 48-53), and, and wherein said array low voltage control circuitry provides said enhanced low operating voltage Vess during all of said active mode (Column 9, lines 48-53), and wherein said array low voltage control circuitry provides said enhanced low operating voltage Vess during all modes (Column 9, lines 48-53), and wherein said array low voltage control circuitry provides said enhanced low operating voltage Mess based on a factor selected from the group consisting a process corner, a transistor parameter, a mode of operation, and a value of a high supply voltage (Figure 1, 9), and wherein said array low voltage control circuitry only provides said lower value for an addressed column of said SRAM array (Figure 8), and wherein said array low voltage control

circuitry employs an active component to provide said enhanced low operating voltage Vess (Figure 8, 10), and wherein said array low voltage control circuitry provides said enhanced low operating voltage Vess employing a component selected from the group consisting of: a diode, transistor, a fuse, a ROM, a voltage regulator, and logic circuitry (Figure 8, 9,10).

Allowable Subject Matter

6. Claims 6-7, 11 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-7, 11 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Tomotani (U.S. Patent No. 6,188,628), and others, does not teach the claimed invention having an array low voltage control circuitry provides the enhanced low operating voltage Vess at higher value when based on a strong n process corner, and Vess at lower value during a read operation than during a write operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2818

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le Primary Examiner Art Unit 2818

THONG LEF
PRIMARY EXAMINER